REMARKS

Applicants have amended the specification and claims in order to correct formal errors and more particularly define the invention taking into consideration the outstanding Official Action. The title has been amended as requested in the Official Action. The amendments to the specification are fully supported by the specification as originally filed and as would be interpreted by one skilled in the art to which the invention pertains. These amendments do not introduce new matter into the application.

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

Response to Rejections Under 35 U.S.C. § 102

Claims 1-3 and 5-6 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,996,070 (Yamada). Claims 1-3, 5-6 and 10-11 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,865,662 (Wang). These rejections are respectfully traversed.

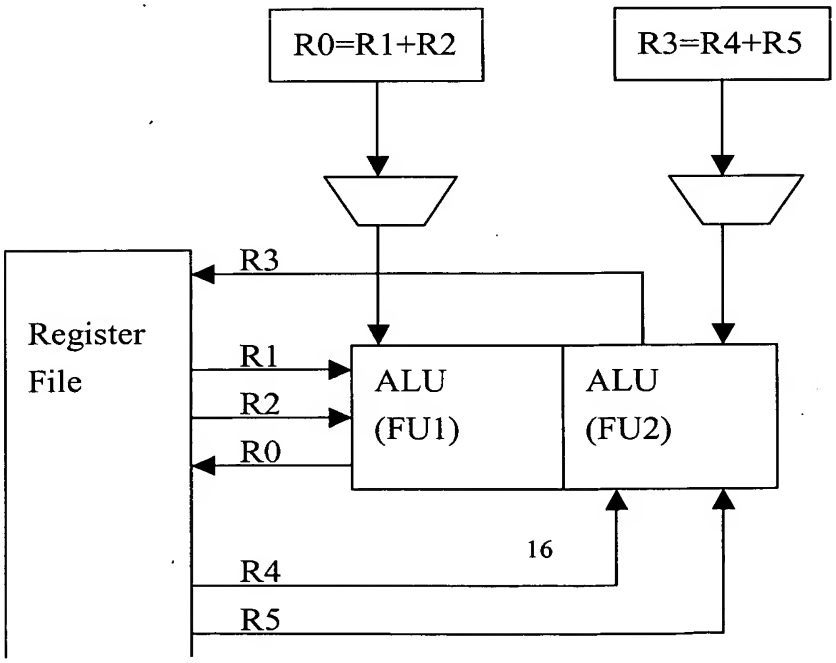
With regard to claims 1-3 and 5-6, Applicants respectfully point out that, in the Yamada patent, the processor structures and the respective execution procedures (Abstract, FIGS. 5, 6, 12, 13 and associated description) use a 3-bit execution condition field 105 (3-bit CC field) to determine whether the execution of the operation_0 in the operation fields 106 and 107, the execution of the operation_1 and the execution of the

operation fields 108, 109 and 110 are valid or invalid based on the status of the F0 and F1 flag bits as execution flags (column 7, lines 54-60), which has the disadvantage discussed in Applicant's specification that the instruction requires a 3-bit condition field, resulting in insufficient bits for encoding an instruction. In contrast, in the present invention, conditional instructions are executed based on a flag, instead of any conditional field embedded in an instruction. Specifically, the flag is set by, for example, a compare instruction, so that when the flag is set to 1, first N-bit instructions following the compare instruction are executed, and when the flag is set to 0, second N-bit instructions following the compare instructions are executed. Therefore, there is no need to have any conditional field embedded in an instruction (such as the 3-bit condition execution condition field 105 of Yamada) to support condition execution, so as not to waste the instruction encoding space thereby increasing the code density. Accordingly, the invention is different from and better than the cited reference.

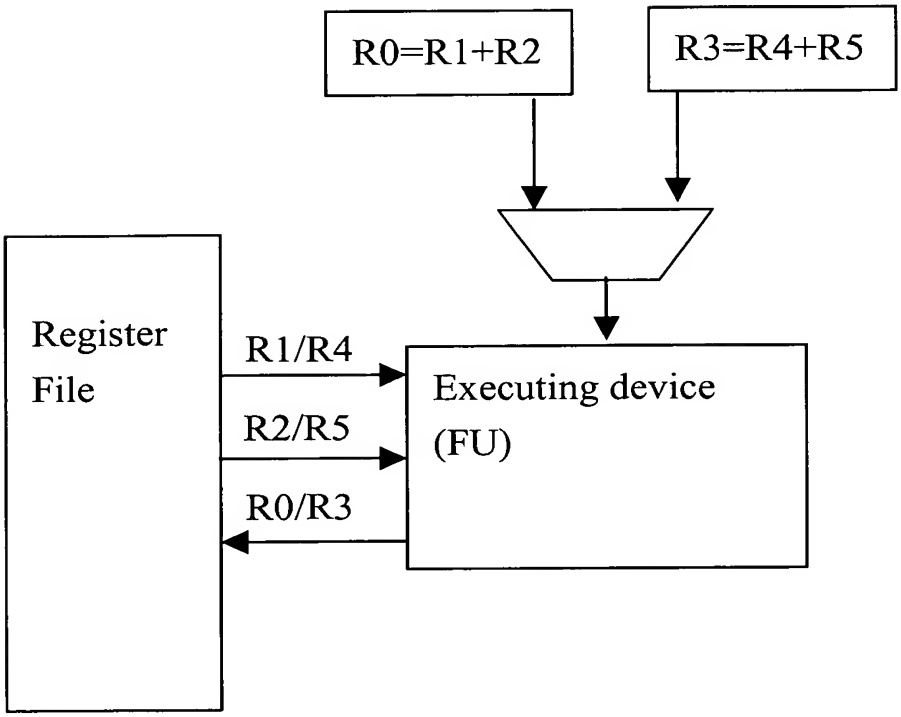
With regard to claims 1-3, 5-6, and 10-11, the Applicants respectfully point out that in the Wang patent the processor structure implements four flags (80a, 80b, 80c, 80d) in a conditional execution head (CEX) as the respective conditional indicators to indicate a condition for the respective instructions or sub-instructions to be executed in the corresponding functional units in parallel (Abstract, Fig. 4 and associated description). These flags (80a, 80b, 80c, 80d) must be provided for the corresponding instructions. That is, flag 80a must be provided for instruction one 82; flag 80b must be provided for instruction two 84; flag 80c must be provided for instruction three 86; and flag 80d must be provided for instruction one 88. Further, these instructions 82, 84, 86,

88 are respectively executed in four different functional units 83, 85, 87, 89. However, in the invention, only one flag is applied (FIG. 3 and associated description), and only one functional unit is required to execute the instruction. This flag is set by a comparison instruction. The subsequent first N-bit instructions are executed by the same instruction executing device 340 (functional unit) if the flag is zero, or the subsequent second N-bit instructions are executed by the same instruction executing device 340 (functional unit) if the flag is not zero (FIG. 5). Therefore, the claimed flag is neither encoded in an instruction nor configured in a conditional execution head. As a result, sufficient bits can be provided for encoding an instruction because no conditional bit is required in each instruction, and no additional hardware, such as conditional execution head (CEX), is required.

Because of this difference between the present invention and the processor disclosed in the Wang patent, a conditional instruction can be more easily implemented by the present invention than by Wang patent. For example, to implement an instruction: if a=0 R0=R1+R2 else R3=R4+R5, the Wang patent needs the following architecture which requires four read ports and two write ports for the register file:



The present invention needs the following architecture which requires only two read ports and one write port for the register file:



Accordingly, when a conditional instruction is executed, the applied structure in the invention is different from that in the Wang patent, and the invention only requires a simpler circuit implementation than the Wang and has the practical advantage due to the lower cost.

Response to Rejections Under 35 U.S.C. § 103

Claims 4 and 7-9 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada, and claims 4 and 7-9 have been rejected under 35 U.S.C. § 103(a) as being

unpatentable over Wang. These rejections are also respectfully traversed.

With regard to all claims above, the applicants respectfully note that, in addition to the description cited above, the values M and N are specially pointed out. This is a must because, as those skilled in the art will appreciate, processors are a hardware-dependence machine. Accordingly, the invention represents and improvement over the cited references.

CONCLUSION

In view of the foregoing remarks, reconsideration and allowance of the application are now believed to be in order, and such action is hereby solicited. If any points remain in issue that the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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